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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,370	08/15/2003	Man Wang	38484-8008US	2543

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EXAMINER	
CHANG, DANIEL D	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/642,370	WANG, MAN	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *9-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5 and 6* is/are rejected.

7)☒ Claim(s) *4,7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restrictions

Applicant's election without traverse of Group I in the reply filed on January 3, 2005 is acknowledged.

Drawings

The drawings are objected to because of a typographical error. In Fig. 3, under OP2, "Cou" appears to be "Cout".

The drawings are objected to as failing to comply with 37 CFR 1.84(i) & 37 CFR 1.84(p) because lines, numbers & letters are not uniformly thick and well defined, clean, durable, and black (poor line quality). Also, some characters are too small.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Ho et al. (US 5,455,525, "Ho" hereinafter).

Regarding claim 1, Ho discloses, at least in Figs. 4 and 6, a field programmable gate array (FPGA) comprising:

an interconnect structure (34, 36) for routing signals on said FPGA; and

a plurality of logic heads (32) that receive a plurality of logic head inputs (60N, 60N, 60E, 60S) from said interconnect structure and output a plurality of logic head outputs (62N, 62N, 62E, 62S) to said interconnect structure, said logic heads comprising:

(1) a plurality of logic blocks (86) that are capable of performing combinatorial logic on said logic head inputs, said plurality of logic blocks formed in a cascaded manner such that the outputs of some logic blocks are provided as inputs to other logic blocks;

(2) an input section (80N, 80N, 80E, 80S) that receives said plurality of logic head inputs and routes said plurality of logic head inputs to said plurality of logic blocks; and

(3) an output section (100) that interfaces to and outputs said logic head outputs to said interconnect structure.

Regarding claim 2, Ho discloses, at least in Figs. 4 and 6, that said interconnect structure is hierarchical (col. 2, lines 1+) and has multiple levels of interconnect routing (see Fig. 1), one of said multiple levels of interconnect routing being a ring structure (36, 34) dedicated for use with communication of logic head inputs and logic head outputs with immediately adjacent logic heads.

Regarding claim 3, Ho discloses, at least in Figs. 4 and 6, that said ring structure includes a plurality of rings (see 36, 34 in fig. 3), each of said plurality of rings associated with a one of said logic head outputs (62N, 62N, 62E, 62S) of said logic head.

Regarding claim 5, Ho discloses, at least in Figs. 4 and 6, that said input section includes inverters (84) that can selectively invert one or more of said plurality of logic head inputs prior to providing said plurality of logic head inputs to said logic blocks (86).

Regarding claim 6, Ho discloses, at least in Figs. 4 and 6, that wherein said inverters are used when one or more of said logic head input signals are switched by a switch (80) that has been programmed.

Allowable Subject Matter

Claims 4, 7-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chaudhary discloses FPGA having logic element carry chains capable of generating wide XOR functions. Bertolet et al. discloses a programmable inverter circuit used in a programmable logic cell.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel D. Chang
Primary Examiner
Art Unit 2819

dc

DANIEL CHANG
PRIMARY EXAMINER